

HIGH FREQUENCY LATCH

ABSTRACT OF THE INVENTION

A high frequency latch comprising a latch and a plurality of buffers coupled to peak load circuitry produces a peak response at a desired frequency of operation as well as isolating each high frequency latch output of a plurality of outputs to substantially reduce the effects of a kickback signal coupled into the latch output. The peaked load circuitry comprises selectable resistive elements and selectable capacitive elements coupled as a high pass filter to change the bias on a saturation region MOSFET configured as an active load. The high pass filter produces positive feedback on the saturation region MOSFET to increase the bias at high frequencies thereby producing an increased response at a desired operating frequency.